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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,723	01/08/2007	Kozo Fujimoto	FUJI:397	3115

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ROSSI, KIMMS & McDOWELL LLP.
20609 Gordon Park Square, Suite 150
Ashburn, VA 20147

EXAMINER	
BREWSTER, WILLIAM M	
ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
05/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,723	FUJIMOTO ET AL.	
	Examiner	Art Unit	
	WILLIAM M. BREWSTER	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *2-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 6-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *090506; 102706; 041707; 060308; 100608; 102408*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1, 6-15 in the reply filed on 22 April 2009 is acknowledged.

Claims 2-5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 22 April 2009.

This election is made FINAL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 7, 9, 11, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petitbon et al., US Publication No. 2002/006685 A1 in view of Tane, JP Publication No. 2001-274201, both from the IDS, this report will rely upon an English translation of Tane, inclosed.

Petitbon teaches:

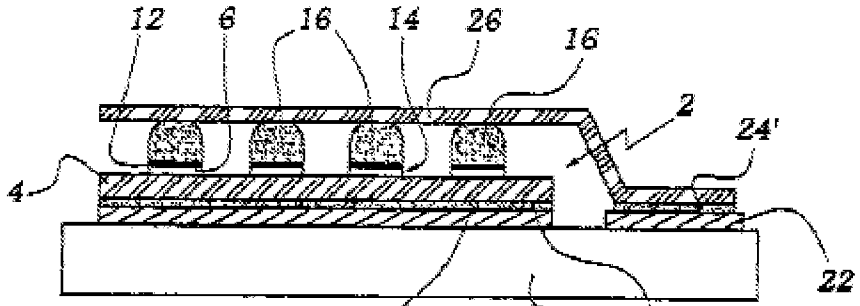


Fig.5

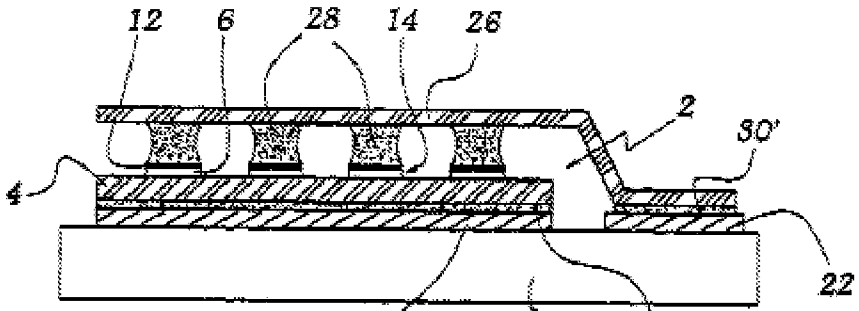


Fig.6

limitations from claim **1. A manufacturing method of a semiconductor module comprising:** in fig. 5, **a first joining step for joining first circuit electrodes** 20 **which are formed on a circuit board** 18 **and back-surface-side die electrodes** not shown **of a semiconductor die** 4 **which forms die electrodes on both front and back surfaces;**

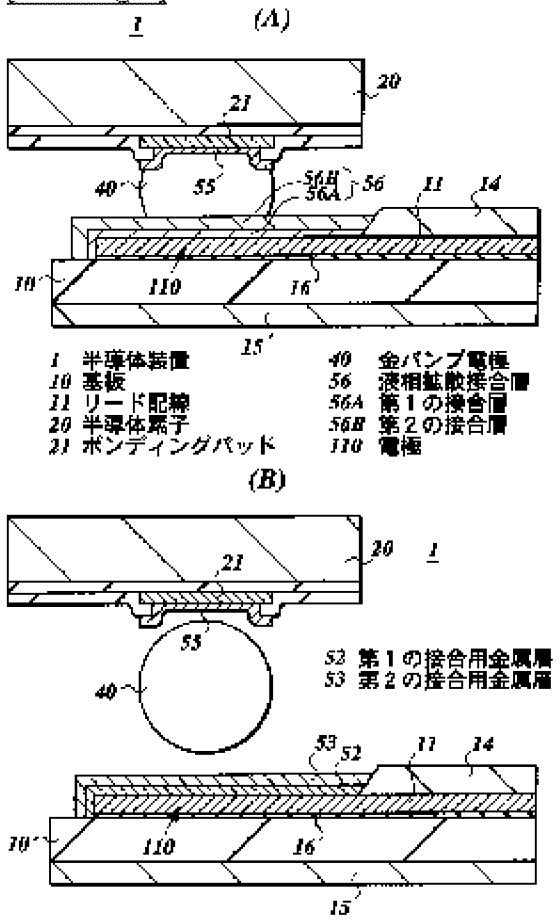
in fig. 6, **a second joining step for joining the front-surface-side die electrodes** 28

of the semiconductor die and one ends of linear or plate-like connecting members 26**; and**

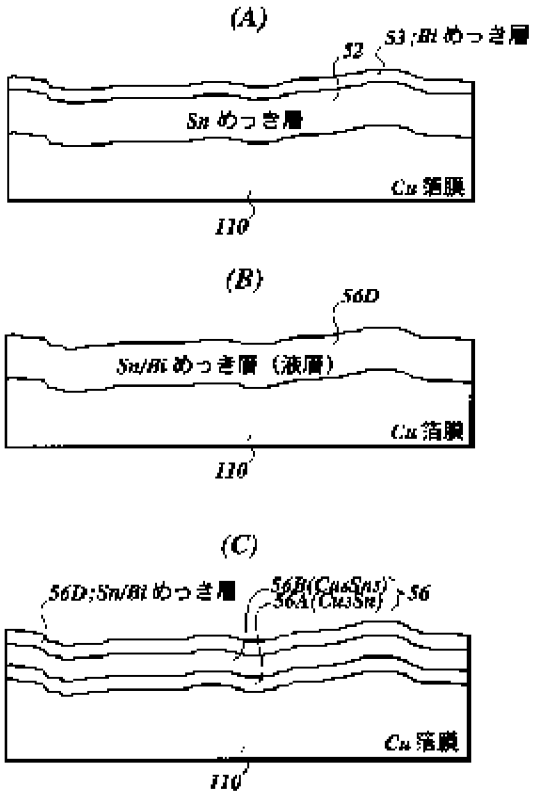
a third joining step for joining another ends of the connecting members and second circuit electrodes which are formed on the circuit board, wherein in at least one of the first joining step, the second joining step and the third joining step, a low-melting-point metal layer 16 **is preliminarily formed on at least one of a pair of conductive portions to be connected with each other and, thereafter, the pair of conductive portions are arranged to face each other and are heated and pressurized at a temperature which melts at least the low-melting-point metal thus diffusing the low-melting-point metal layer into the pair of conductive portions by whereby the pair of conductive portions are joined to each other**, p. 2, ¶ 42 - p. 3, ¶ 39.

Petitbon does not specify using solid-liquid diffusion for bonding, but Tane does. Tane teaches:

[Drawing 1]


1
(A)
20
21
40
55
56H
56A
56
11
14
10
110
16
15
1 半導体装置
10 基板
11 リード配線
20 半導体素子
21 ボンディングパッド
40 金バンプ電極
56 液相拡散接合層
56A 第1の接合層
56B 第2の接合層
110 電極
(B)
20
1
21
55
40
53 第1の接合用金属層
53 第2の接合用金属層
53
52
11
14
10
110
16
15

[Drawing 3]



limitations from claim **1. A manufacturing method of a semiconductor module comprising:** in fig. 1, **a joining step for joining first circuit electrodes** 110 **which are formed on a circuit board and back-surface-side die electrodes of a semiconductor die** 21 **which forms die electrodes on both front and back surfaces;**

the second joining step and the third joining step, a low-melting-point metal layer 52, 53 **is preliminarily formed on at least one of a pair of conductive portions to be connected with each other and, thereafter, the pair of conductive portions are arranged to face each other and are heated and pressurized at a temperature** in

fig. 3, **which melts at least the low-melting-point metal thus diffusing the low-melting-point metal layer into the pair of conductive portions by solid-liquid diffusion whereby the pair of conductive portions are joined to each other**, ¶ 34-38;

6. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, wherein the low-melting-point metal layer contains at least one selected from a group consisting of SnIn, In, Bi, SnBi, ¶ 36;

7. A manufacturing method of a semiconductor module according to claim 6, wherein a heating temperature at the time of the joining is a temperature which is 0 to 100°C higher than the melting point of the low-melting-point metal, ¶ 38;

9. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, wherein a material of the pair of conductive portions 110 **is one selected from a group consisting of Cu, Ni, Au, Al or alloy thereof,** ¶ 35;

11. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, in fig. 3, **wherein the heating-and-pressurizing is performed until the low-melting-point metal layer forms an intermediate alloy** 56 **layer between the pair of conductive portions,** ¶ 35;

13. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, in fig. 3, **wherein the surfaces of the pair of conductive portions are formed of coarse surfaces having the surface roughness Ra of 0.4 to 10 μm.**

While Tane does not specify the exact dimensions of the surface roughness, it is reasonable to assume they are within the claimed limitations. Further, the practitioner may optimize the ranges.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art . . . such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality . . . More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

> In re Aller 105 USPQ 233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another

variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Also see MPEP §§2144.04 IV. *Changes in Size, Shape, or Sequencing of Adding Ingredients* and 2144.05 II. *Optimiztion of Ranges*.

Tane further teaches:

14. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, in fig. 1, **wherein the low-melting-point metal layer is formed such that at least two kinds of metals which can form alloy are stacked in two layers** 52, 53 **or more,** in fig. 3, **and the stacked metal layers are preheated to make the metal layers react with each other to form an alloy layer**, ¶ 38.

Tane gives motivation in ¶ 38. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Tane's process with Petitbon's invention would have beneficial because it forms strong bonds.

Claims 8, 10, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petitbon in view of Tane as applied to claim 1 above, and further in view of Abys, US Patent No. 5,360,991.

Petitbon and Tane do not specify a very thin bonding layer, but Abys does. Abys teaches:

8. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, in fig. 3, **wherein a total thickness of the low-melting-point metal layer** 24 **which is formed preliminarily between the pair of conductive portions assumes a value which falls within a range from 0.1 to 1 μm**, col. 4, lines 2-21;

10. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, wherein the heating-and-pressurizing is performed until the low-melting-point metal layer is completely diffused in the pair of conductive portions by solid-liquid diffusion, wherein by virtue of the thin bonding layer, this will occur;

12. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, in fig. 1, **wherein the connection member is a lead frame** 10, co.. 2, lines 51-58.

Abys gives motivation in col. 1, lines 36-48. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Abys's process with Petitbon's and Tane's invention would have beneficial because it helps prevent cracking.

Claims 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Petitbon in view of Tane as applied to claim 1 above, and further in view of Karasawa, JP Publication No. 05-009713, from the IDS.

Petitbon and Tane do not specify vapor-depositing, but Karaswa does. Karasawa teaches:

15. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, wherein the low-melting-point metal layer is formed by vapor-depositing alloy which constitutes an evaporation source and, at the time of performing the vapor deposition, an evaporation pressure ratio in reaction steps of respective metal components of the alloy is controlled thus forming a film having the target alloy composition, PURPOSE and CONSTITUTION, the ratios and coefficient are thus controlled to form the desired film;

16. A manufacturing method of a semiconductor module according to any one of claims 1, 2, 4 and 5, wherein the low-melting-point metal layer is formed by vapor-depositing alloy which constitutes an evaporation source and, at the time of performing the vapor deposition, a product of an evaporation pressure ratio and an active coefficient ratio in reaction steps of respective metal components of the alloy is controlled thus forming a film having the target alloy composition, PURPOSE and CONSTITUTION, the ratios and coefficient are thus controlled to form the desired film.

Karasawa gives motivation in col. 1, lines 36-48. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Karasawa's process with Petitbon's and Tane's invention would have beneficial because the practitioner need not worry about the deposition rate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM M. BREWSTER whose telephone number is (571)272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

9 May 2009

/William M. Brewster/
Primary Examiner, Art Unit 2823